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328875(28)

B. E. (Eight Semester) Examination, April-May 2020

(Old Scheme)

(Et & T Engg. Branch)

MICRO-ELECTRONIC DEVICES & VLSI TECHNOLOGY

(Elective-III)

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note *: All questions carry equal marks. Part (a) of each question is compulsory. Attempt any* ***two*** *from (b), (c) & (d).*

Unit-I

1. (a) What do you mean by scale of Integration. Give the classification. 2

(b) Why CZ techniques is preferred over the other techniques in silicon processing. 7

(c) Give comparitive analysis of Bridgeman Technique and Float Zone process. 7

(d) Explain the process of silicon wafer preparation. 7

Unit-II

2. (a) Give the types of Oxidation process. 2

(b) Show that to grow an oxide layer of thickness x, a thickness of 0·44 x of silicon is consumed. 7

(c) Explain Dielectric Deposition with neat diagram. 7

(d) Explain Polysilicon Deposition in detail. 7

Unit-III

3. (a) Define the Fick's diffusion law. 2

(b) Draw & explain the ion implantation system. Also explain the role of mass separator & Beam scanning in detail. 7

(c) Which implantation techniques avoids long diffusion steps. Explain the terms implantation damage. channeling & recoils. 7

(d) Explain Vacancy mechanism & Interstitial mechanism. 7

Unit-IV

4. (a) Define EPITAXY & give its uses in MOS structure. 2

(b) (i) Explain optical Lithography with neat diagram. 5

(ii) A proximity printer operates with a 20 m marks of wafer gap and a wavelength of 250 nm. Find line width that can be obtained. 2

(c) Give comparison between WET & DRY ETCHING. 7

(d) Explain the flow diagram of process simulation and Integration. 7

Unit-V

5. (a) Draw MOSFET structure. 2

(b) Explain the operation of *N* channel MOSFET with pictorial view. 7

(c) Explain following :

(i) Channel Length Modulation 3½

(ii) Subthreshold Region 3½

(d) Explain scaling of MOSFET. 7